

SSD2386 HIGH-INTEGRATED HMI CONTROLLER

PRODUCT BRIEF

CHIP OVERVIEW

The SSD2386 is a feature-rich, highly integrated, low power product, suitable for HMI, mobile, and battery device, as well as high-resolution intelligent application.

The SSD2386 includes a 64-bit quad-core processor, high performance H.265/H.264/MJPEG video encoder, Intelligence Processing Unit (IPU) as well as high speed I/O interfaces like USB, Ethernet, and 12-bit ADC. These features in combination make the SSD2386 an ideal solution that facilitates design and development of high-performance, high-picture-quality, and low-cost products.

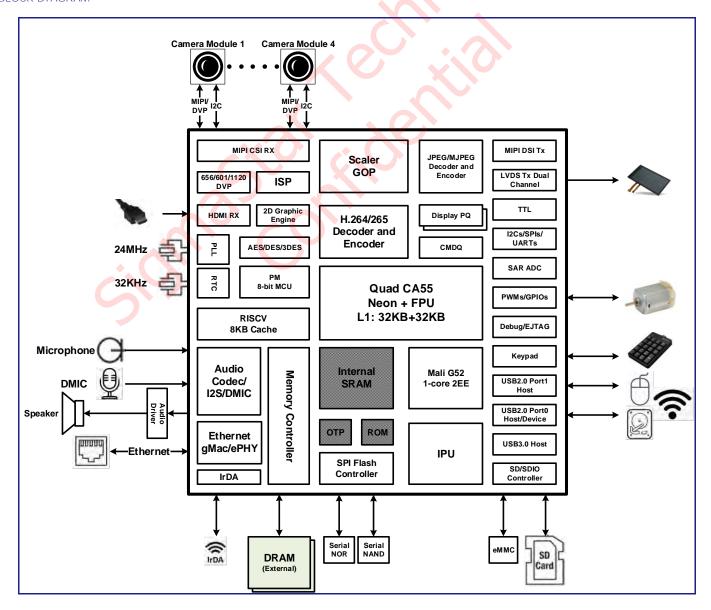
The programmable neural network inference engine featured in the SSD2386 allows customers to achieve a rich variety of intelligent applications with ease.

Implemented with the quad-core ARM Cortex-A55 CPU as well as an IPU, the SSD2386 enables fast startup, real-time performance, and connections with various peripheral interfaces.

Efficient computing resources are available to help customers develop industry and consumer applications. Advanced low-power, low-voltage architecture and optimized design flow are implemented to fulfill long time usage applications. Hardwired AES/DES/3DES cipher engines are integrated to support secure boot, authentication, and video/audio stream encryption in security system.

The SSD2386, powered by SigmaStar Technology, comes with a complete hardware platform and software SDK, allowing customers to speed up "Time-to-Market."

BLOCK DIAGRAM





FEATURES

High Performance Processor Core • ARM Cortex-A55 Quad Core

- 32KB L1 I-cache and 32KB L1 D-cache for each core
- 128KB L2 cache for each core and 512KB L3 cache Neon and FPU
- Separate power domain for each core Stand-alone voltage domain

Video Input Interface

- Supports 8/10/12-bit parallel interface for raw data input Supports 8-bit CCIR656/601 interface Supports 16-bit BT1120 interface

- . Supports MIPI interface with 6 data lanes and 4 clock
- Supports sensor interface with both parallel and MIPI
 Supports max. 6M (2688x2564) pixels video recording and image snapshot
- Supports HDMI Rx 1.4b with HDCP1.4
 Static and adaptive bad pixel compensation
- Crosstalk noise reduction
 Temporal-domain Noise Reduction (3DNR)
- Sharpening filters for image enhancement
 Spatial-domain Noise Reduction (2DNR) for luma and chroma image

- chroma image
 Filter to remove purple false color in highlight regions
 Optical black correction
 Symmetric/Asymmetric lens shading compensation
 Auto White Balance (AWB) / Auto Exposure (AE) / Auto Focus (AF)
- CFA color interpolation and demoire filter Color correction and color adjustment engine
- Gamma correction
 High Dynamic Range (HDR) with two exposure frames and de-ghost function
- Frame buffer data compression and de-compression to save memory bandwidth
- Wide Dynamic Range (WDR) with local tone mapping Flip, Mirror, and Rotation with 90 or 270 degree
- Fully programmable multi-function scaling engines

- H.265/HEVC Encoder
 Supports max. 4K30fps
 Fully compatible with ISO/IEC 23008-2 High Efficiency video coding Main Profile, Level 5.0 encode

- Supports I-frame and P-frame Supports resolution from 256x128 to 4096x4096
- 549-5013 Testing Francision motion vectors
 Deblocking filter and Sample Adaptive Offset (SAO)
 Picture/CTU/subCTU level rate control
- Region of Interest (ROI) encoding with custom OP map
 H.264/AVC Encoder
 Supports max. 4K30fps

- Compatible with the ITU-T Recommendation H.264 specification
- Baseline/Constrained Baseline/Main/High Profile, Level 5.1 encode
- Supports resolution from 256x128 to 4096x4096
- 1/4-pixel precision motion vectors In-loop deblocking filter CABAC/CAVLC support Error resilience tools

- Frame level and MB level rate control
- Region of Interest (ROI) encoding with custom QP map
- Region of Interest (ROI) encoding with custom OP map
 H.265/HEVC Decoder

 Supports max. 4K30fps decode
 Fully compatible with ISO/IEC 23008-2 High Efficiency
 Video Coding Main Profile
 HEVC Main Profile, Level 5.0 decode
 Supports resolution from 176x128 to 4096x4096
 I/P/B slices

 - Prediction Unit (PU): 64x64 to 4x4 Transform Unit (TU): 32x32 to 4x4

 - 1/4 motion compensation with 8-tap filters High performance CABAC decoding

 - In-loop deblocking filtering
 Sample adaptive offset (SAO)
 Error concealment

H.264/AVC Decoder

- Supports max. 4K30fps decode
 Compatible with the ITU-T Recommendation H.264 specification
- Baseline/Constrained Baseline/Main/High Profile. Level 5.1.
- Supports resolution from 176x128 to 4096x4096 Variable block size (16x16, 16x8, 8x16, 8x8, 8x4, 4x8 and 4x4)
- CABAC/CAVLC support
- In-loop deblocking filter
- Error detection, concealment and error resilience tools

- JPEG/MJPEG Encoder/Decoder
 JPEG/MJPEG baseline encoding and decoding
 Supports YUV422 or YUV420 input formats, YUV422 output formats Max. 8192x8192 frame resolution

- 1080p60 for encoding and decoding max. performance Supports real-time mode and frame encode mode

3D Graphic Engine

- Mali G52 1-core 2EE with 64KB Cache Supports IFC Supports OpenGL ES 1.1, 2.0, and 3.2
- Supports Vulkan 1.0 and 1.1 Supports OpenCL 2.0 Full Profile
- Supports 1200Mpix/s fill rate when operating at 600MHz clock frequency
- Supports 28.8 GFLOPs when operating at 600MHz clock frequency

Intelligence Processing Unit (IPU) • Pure hardwired accelerator

- Programmable 4/8/16-bit process Supports RGB/YUV data format R/W DMA
- Supports NGD/TOV data offine NW DIMA Stand-alone voltage domain Supports various video analysis functions like FD/FR, human detection, MD/OD, object tracking, etc.
- Supports median filter for TOF Supports 2D TOF filter

Co-Processor (RISCV)

- Supports RV32 base instruction set, and M/C extension 6 Stage Pipeline, Single Issue, in-order dispatch, out-of-order execution
- 8KB i-cache and 8KB d-cache Up to 466MHz clock rate

- Supports dynamic branch prediction Supports memory property configuration
- Supports JTAG debug
- Co-Processor (8-bit MCU)

 Located in PM power domain
- Supports 8KB internal PSRAM
- Supports XDATA SRAM size up to 512Byte Internal FRO clock up to 48MHz

Audio Processor

- Supports 3-channel ADC with single-end or differential mode
- Supports 2-channel DAC with single-end mode

- Supports 2-chainer DAC with single-end mode
 ADC and DAC SNR over 96dB
 Digital and analog gain adjustment
 Supports 8-CH DMIC (1 clock + 4 data)
 Supports 1250 TDM mode with input max. 8-ch and output
- 2-cn Supports I2S1 2-ch input and 2-ch output I2S0/1 support Master or Slave mode and 4/6 wire mode Supports HDMI RX with 2 channels Supports SPDIF 2 channels
- Video Output Interface

- ideo Output Interface
 Dual read DMAs and display channels
 Picture quality enhancement (gamma, AWB, contrast,
 saturation, sharpness, brightness, 3x3 matrix)
 Each display channel can output to MIPI/LVDS/Digital
 port, digital port including one of TTL/CCIR601/656
 Supports MIPI DSI TX, RGB 16/18/24-bit,
 2560x1600@60fps
 TTL/(Partial) BCB interface 14/44 bit 1400 700 700 500

- 2500x1600@60lpS TTL/Parallel-RGB interface, 16/24-bit, 1280x720@60fps Supports LVDS TX dual channel, up to 1080@60fps Simultaneous output display for MIPI/LVDS/Digital port Scale-down and write-back DMA

- Advanced Color Engine
 Luma gain/offset adjustment
- Supports 2D peaking with user definition filter Horizontal noise masking
- Local Contrast Enhancement (LCE)
- Direct Luma Correction (DLC)
 Black/White Level Extension (BLE/WLE)
- IHC/ICC/IBC for hue, saturation, brightness and favorite color adjustment
- Histogram statistics

- SPI NOR/NAND Flash Interface

 Compliant with standard, dual and quad SPI flash memory components
 • Max. 108MHz clock rate

- SD/eMMC Interface

 SD card 2.0 x1 and SD card 3.0 (SDR104 or
- SDR50/DDR50) x1, data bus 1/4-bit mode SDIO 2.0 (SDR25) x1, data bus 1/4-bit mode eMMC 5.0 with 4/8 data bit and max. 200MHz clock rate, HS400 DDR mode
- USB Interface
- USB3.0 Host
- USB2.0 port0 configurable Host or Device USB2.0 port1 Host
- Host mode supports EHCI specifications

- DRAM Memory
 External 16-bit x2 or 32-bit x1 DDR4/DDR3/DDR3L/LPDDR4/LPDDR3
- Supports memory space up to 32Gb Data rate up to 2133Mbps for DDR3, 3200Mbps for DDR4, and 2666Mbps for LPDDR4

- Connectivity

 Built-in 10/100/1000M Ethernet MAC with RGMII/RMII
- Built-in 10/100M Ethernet MAC and Ethernet PHY
- Hash table with 256 entries Broadcast/Multicast storm prevention
- Supports both full-duplex and half-duplex operation Supports IEEE 802.1Q VLAN tag detection for reception
- Supports checking IPv4 header checksum and TCP, UDP,
- or ICMP checksum encapsulated in IPv4 or IPv6 datagram Supports TCP Segmentation Offload (TSO) and UDP Fragmentation Offload (UFO)
- GigaMAC supports IEEE1588v2 PTP GigaMAC supports IEEE802.1 QoS

- Supports AES128/AES192/AES256/DES/ 3DES/RSA2048/SHA-1/SHA-256
 Supports secure booting

- FIPS 140-1 compliant random number generator Embedded OTP (One Time Programmable) memory to store secure and calibration data
- Boot Options
 SPI NOR

 - SPI NAND with ECC
 - SD Card eMMC
- USB
- Peripherals

 Dedicated GPIOs for system control Supports 8x PWM inputs¹ and 20x PWM outputs (shared
- with GPIOs) Up to six generic UARTs and one fast UART with flow
- control
- Three generic timers and one watchdog timer
 Two SPI interfaces, which can be configured as master or slave mode
- Up to six I2C Masters
- Built-in 10-bit SAR ADC with 2-channel analog inputs for different kinds of application Built-in 12-bit SAR ADC with 24-channel analog inputs for
- different kinds of application Supports 7x7 Keypad
- Supports IrDA Supports POR (Power On Reset) Supports internal temperature sensor
- Real Time Clock (RTC)

 Built-in RTC working with 32.768 KHz crystal

 Alarm interrupt for wakeup

 Tick time interrupt (millisecond)

 Built-in regulator
- Supports low leakage RTC mode for long battery
- application Always on power domain (PM)
- Built-in LDO to provide both 0.9V and 1.8V power sources Built-in RC FRO to generate clock source Supports 8-bit MCU to controll PM GPIO
- Supports multiple GPIOs for power control and RTC events
- Package
 BGA 19x19 Ball pitch and size: 0.65 and 0.3 mm

4 or 6 Layer PCBMoisture Sensitivity Level (MSL): 3

^{1 8-}ch for duty measurement and 4-ch for pulse counting