Sigm Star SSU9386 High Performance AIOT System-on-Chip Product Brief

CHIP OVERVIEW

The SSU9386 is a feature-rich, highly integrated, low power product, suitable for AIoT, mobile, and battery device, as well as high-resolution intelligent application.

The SSU9386 includes a 64-bit quad-core processor, high performance H.265/H.264/MJPEG video encoder, Intelligence Processing Unit (IPU) as well as high speed I/O interfaces like USB, Ethernet, and 12-bit ADC. These features in combination make the SSU9386 an ideal solution that facilitates design and development of high-performance, high-picture-quality, and low-cost products.

The programmable neural network inference engine featured in the SSU9386 allows customers to achieve a rich variety of intelligent applications with ease.

Implemented with the quad-core ARM Cortex-A55 CPU as well as an IPU, the SSU9386 enables fast startup, real-time performance, and connections with various peripheral interfaces.

Efficient computing resources are available to help customers develop industry and consumer applications. Advanced low-power, low-voltage architecture and optimized design flow are implemented to fulfill long time usage applications. Hardwired AES/DES/3DES cipher engines are integrated to support secure boot, authentication, and video/audio stream encryption in security system.

The SSU9386, powered by SigmaStar Technology, comes with a complete hardware platform and software SDK, allowing customers to speed up "Timeto-Market."

BLOCK DIAGRAM



FEATURES

- High Performance Processor Core ARM Cortex-A55 Quad Core

 - 32KB L1 I-cache and 32KB L1 D-cache for each core
 - 128KB L2 cache for each core and 512KB L3 cache
 - Neon and FPU
 - Separate power domain for each core
 - Stand-alone voltage domain
 - Video Input Interface
 - Supports 8/10/12-bit parallel interface for raw data input
 - Supports 8-bit CCIR656/601 interface
 - Supports 16-bit BT1120 interface · Supports MIPI interface with 6 data lanes and 4
 - clock lanes · Supports sensor interface with both parallel and MIPI
 - Supports max. 6M (2688x2564) pixels video recording and image snapshot
 - · Static and adaptive bad pixel compensation
 - Crosstalk noise reduction
 - Temporal-domain Noise Reduction (3DNR)
 - Sharpening filters for image enhancement
 - Spatial-domain Noise Reduction (2DNR) for luma and chroma image
 - · Filter to remove purple false color in highlight regions
 - Optical black correction
 - Symmetric/Asymmetric lens shading compensation
 - Auto White Balance (AWB) / Auto Exposure (AE) / Auto Focus (AF)
 - CFA color interpolation and demoire filter
 - Color correction and color adjustment engine Gamma correction
 - High Dynamic Range (HDR) with two exposure frames and de-ghost function
 - Frame buffer data compression and decompression to save memory bandwidth
 - Wide Dynamic Range (WDR) with local tone mapping Flip, Mirror, and Rotation with 90 or 270 degree
 - Fully programmable multi-function scaling engines
 H.265/HEVC Encoder

 - H.265/HEVC Encoder Supports max. 4K@30fps Fully compatible with ISO/IEC 23008-2 High Efficiency video coding Main Profile, Level 5.0 encode Supports I-frame and P-frame Supports resolution from 256x128 to 4096x4096

 - 1/4-pixel precision motion vectors

 - Deblocking filter and Sample Adaptive Offset (SAO)

 - Picture/CTU/subCTU level rate control
 Region of Interest (ROI) encoding with custom QP map
- map H.264/AVC Encoder Supports max. 4K@30fps Compatible with the ITU-T Recommendation H.264 specification
 - Baseline/Constrained Baseline/Main/High Profile,
 - Level 5.1 encode Supports resolution from 256x128 to 4096x4096
 - 1/4-pixel precision motion vectors
 - In-loop deblocking filter •
 - CABAC/CAVLC support
 - Error resilience tools
 - Frame level and MB level rate control
 - · Region of Interest (ROI) encoding with custom QP
- map JPEG/MJPEG Encoder/Decoder
 - JPEG/MJPEG baseline encoding and decoding
 - Supports YUV422 or YUV420 input formats,
 - YUV422 output formats
 - Max. 8192x8192 frame resolution
 - 1080p60 for encoding and decoding max performance

8-ch for duty measurement and 4-ch for pulse counting

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Supports real-time mode and frame encode mode

Intelligence Processing Unit (IPU)

- Pure hardwired accelerator
- Programmable 4/8/16-bit process
- Supports RGB/YUV data format R/W DMA
- Stand-alone voltage domain
- Supports various video analysis functions like FD/FR, human detection, MD/OD, object tracking, etc

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DRAM Memory • External 16-bit x2 or 32-bit x1

Hash table with 256 entries

RGMII/RMII

operation

Security Engines

Boot Options

SPI NOR SPI NAND with ECC

SD Card

Peripherals

(shared with GPIOs)

master or slave mode

flow control

• eMMC

USB

reception frames

IPv4 or IPv6 datagram

DDR4/DDR3/DDR3L/LPDDR4/LPDDR3

for DDR4, and 2666Mbps for LPDDR4 Connectivity • Built-in 10/100/1000M Ethernet MAC with

Broadcast/Multicast storm prevention

UDP Fragmentation Offload (UFO)

GigaMAC supports IEEE1588v2 PTP

Supports AES128/AES192/AES256/DES/

Dedicated GPIOs for system control

Supports 8x PWM inputs¹ and 20x PWM outputs

Up to six generic UARTs and one fast UART with

Three generic timers and one watchdog timer Two SPI interfaces, which can be configured as

master or slave mode
Up to six 12C Masters
Built-in 10-bit SAR ADC with 2-channel analog inputs for different kinds of application
Built-in 12-bit SAR ADC with 24-channel analog inputs for different kinds of application
Supports 7x7 Keypad
Supports IrDA
Supports POR (Power On Reset)
Supports internal temperature sensor

Supports internal temperature sensor

Alarm interrupt for wakeup

Always on power domain (PM)

Built-in regulator

application

RTC events

4 or 6 Layer PCB

• BGA 19x19

Package

sources

Tick time interrupt (millisecond)

Real Time Clock (RTC) • Built-in RTC working with 32.768 KHz crystal

Supports low leakage RTC mode for long battery

Built-in LDO to provide both 0.9V and 1.8V power

Supports multiple GPIOs for power control and

2 of 2

Built-in RC FRO to generate clock source

Supports 8-bit MCU to controll PM GPIO

• Ball pitch and size: 0.65 and 0.3 mm

• Moisture Sensitivity Level (MSL): 3

GigaMAC supports IEEE802.1 QoS

3DES/RSA2048/SHA-I/SHA-256

Supports secure booting

Supports both full-duplex and half-duplex

Supports IEEE 802.1Q VLAN tag detection for

Supports checking IPv4 header checksum and TCP, UDP, or ICMP checksum encapsulated in

Supports TCP Segmentation Offload (TSO) and

FIPS 140-1 compliant random number generator

Embedded OTP (One Time Programmable)

memory to store secure and calibration data

Data rate up to 2133Mbps for DDR3, 3200Mbps

Built-in 10/100M Ethernet MAC and Ethernet PHY

• Supports memory space up to 32Gb

- Supports median filter for TOF
- Supports 2D TOF filter
- Co-Processor (RISCV)
- Supports RV32 base instruction set, and M/C extension
- 6 Stage Pipeline, Single Issue, in-order dispatch, out-of-order execution
- 8KB i-cache and 8KB d-cache
- Up to 466MHz clock rate
- Supports dynamic branch prediction
- Supports memory property configuration
- Supports JTAG debug Co-Processor (8-bit MCU)
- Located in PM power domain
- Supports 8KB internal PSRAM
- Supports XDATA SRAM size up to 512Byte
- Internal FRO clock up to 48MHz
- Audio Processor
- Supports 3-channel ADC with single-end or differential mode
- Supports 2-channel DAC with single-end mode
- ADC and DAC SNR over 96dB
- Digital and analog gain adjustment Supports 8-CH DMIC (1 clock + 4 data) Supports I2S0 TDM mode with input max. 8-ch
- and output 2-ch
- Supports I2S1 2-ch input and 2-ch output I2S0/1 support Master or Slave mode and 4/6
- wire mode
- Supports SPDIF 2 channels Video Output Interface

- Dual read DMAs and display channels
 Picture quality enhancement (gamma, AWB, contrast, saturation, sharpness, brightness, 3x3 matrix)
- Each display channel can output to MIPI/ Digital port, digital port including one of TTL/CCIR601/656
- Supports MIPL DSI TX, RGB 16/18/24-bit, 2560x1600@60fps TTL/Parallel-RGB interface, 16/24-bit, 1290y700000
- TTL/Parallet-roop interface, i.e. 2
 1280x720@60fps
 Simultaneous output display for MIPI/Digital port
 Scale-down and write-back DMA
 Advanced Color Engine
 Luma gain/offset adjustment
 Currents 2D peaking with user definition filter

- Supports 2D peaking with user definition filter
- Horizontal noise masking

Compliant with standard, dual and quad SPI flash

SD card 2.0 x1 and SD card 3.0 (SDR104 or

SDR50/DDR50) x1, data bus 1/4-bit mode

USB2.0 port0 configurable Host or Device

SDIO 2.0 (SDR25) x1, data bus 1/4-bit mode

eMMC 5.0 with 4/8 data bit and max. 200MHz

Host mode supports EHCI specifications

- Local Contrast Enhancement (LCE)
- Direct Luma Correction (DLC) Black/White Level Extension (BLE/WLE) IHC/ICC/IBC for hue, saturation, brightness and

favorite color adjustment

SPI NOR/NAND Flash Interface

clock rate, HS400 DDR mode

Histogram statistics

memory components

Max. 108MHz clock rate

SD/eMMC Interface

USB Interface

• USB3.0 Host

USB2.0 port1 Host